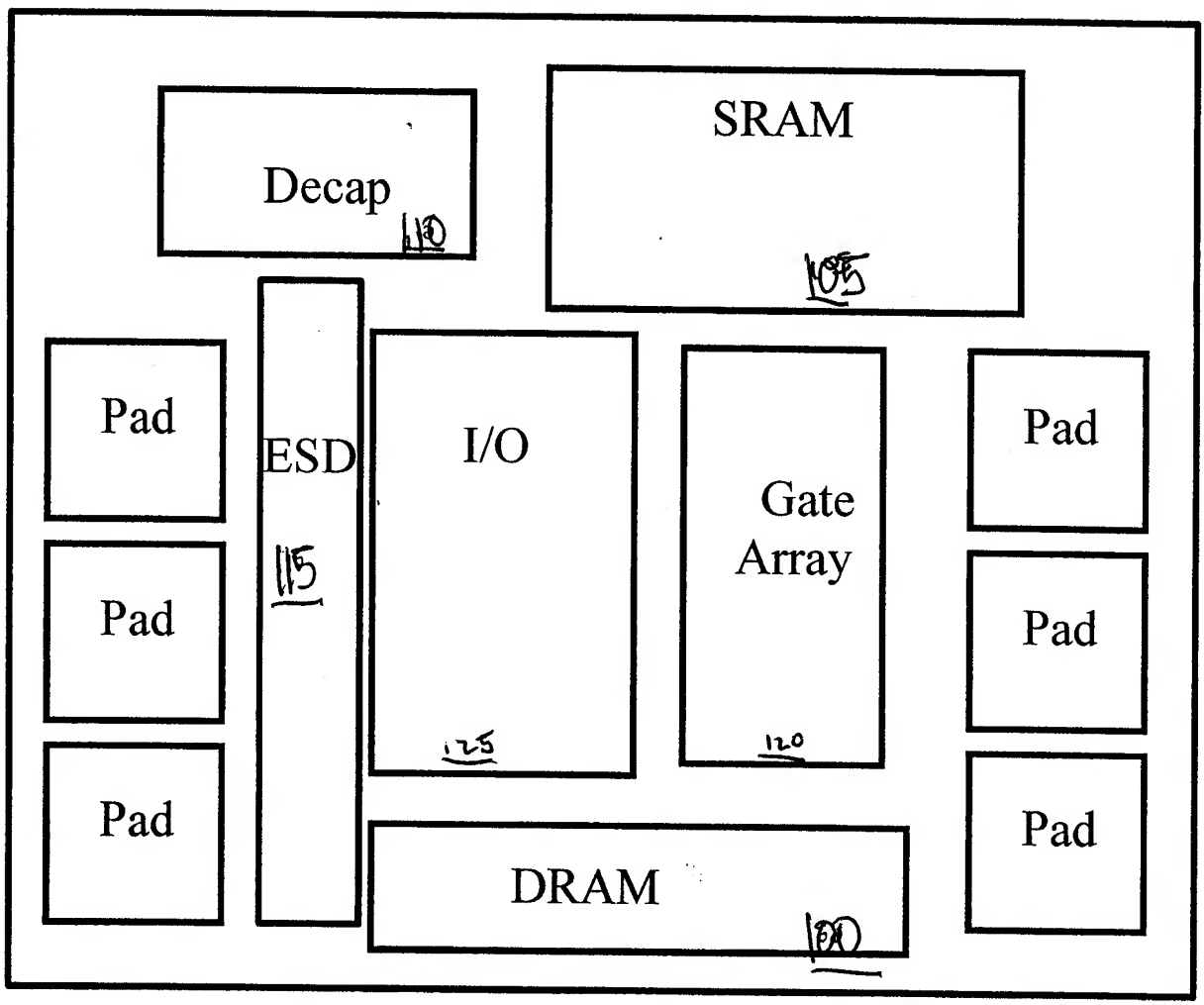
Decap
110
SRAM
105
Pad
Pad
Pad
ESD
115
I/O
125
Gate
Array
120
Pad
Pad
Pad
DRAM
100

Figure 1

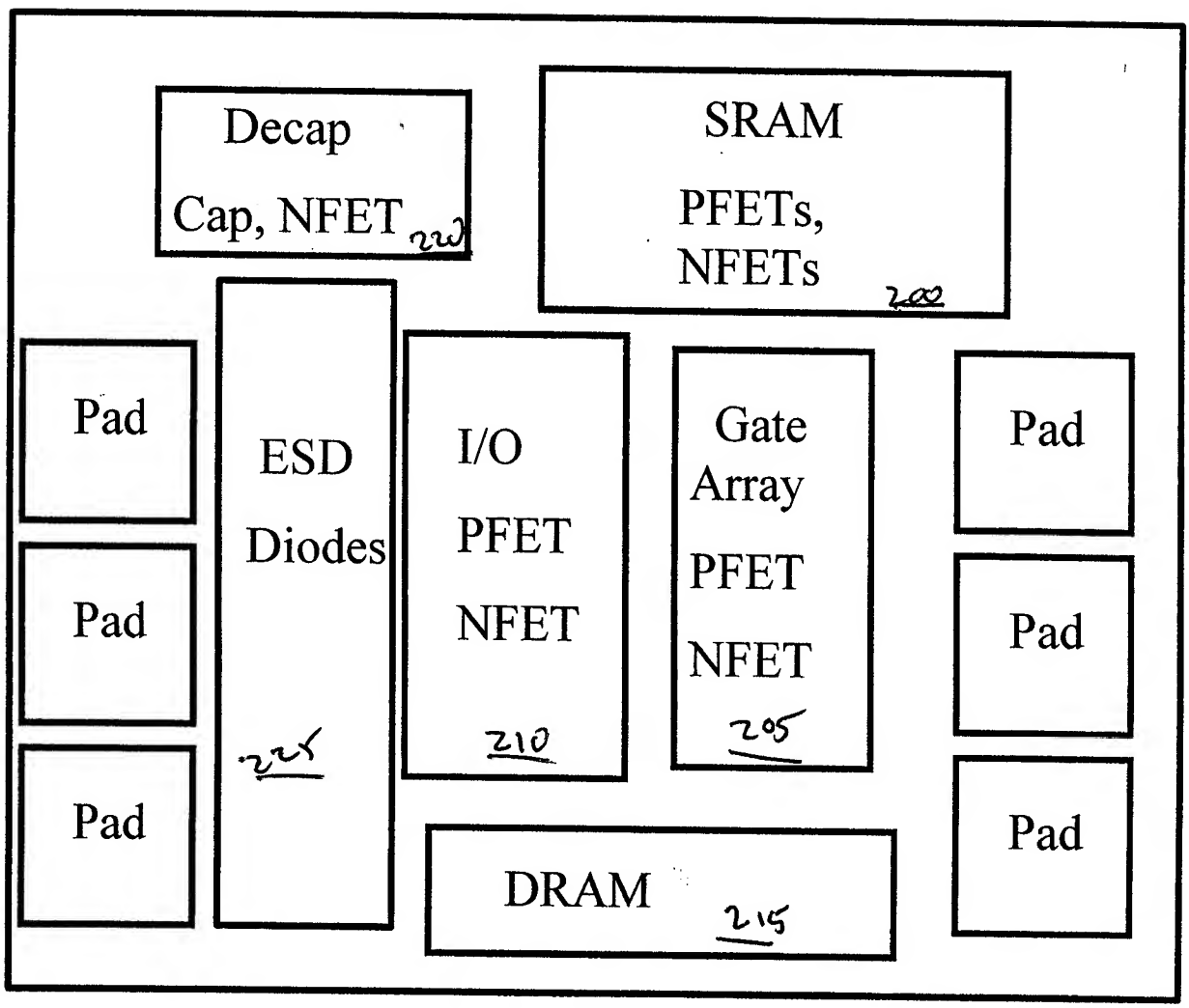
Decap
Cap, NFET
220
SRAM
PFETs,
NFETs
200
Pad
Pad
Pad
ESD
Diodes
225
I/O
PFET
NFET
210
Gate
Array
PFET
NFET
205
Pad
Pad
Pad
DRAM
215

Figure 2

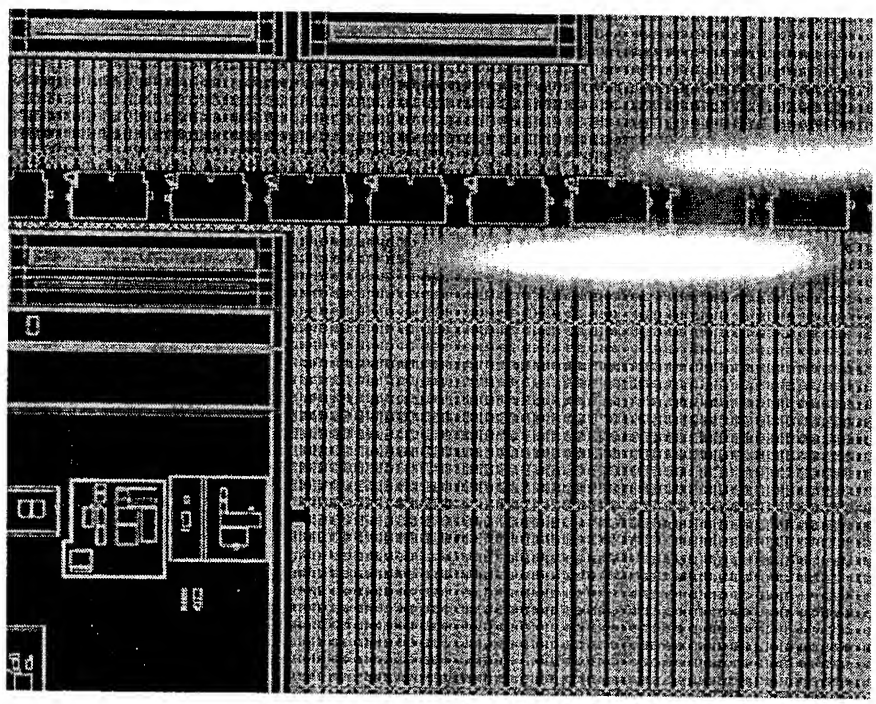

Figure 3. Propagation of Latchup from book to book

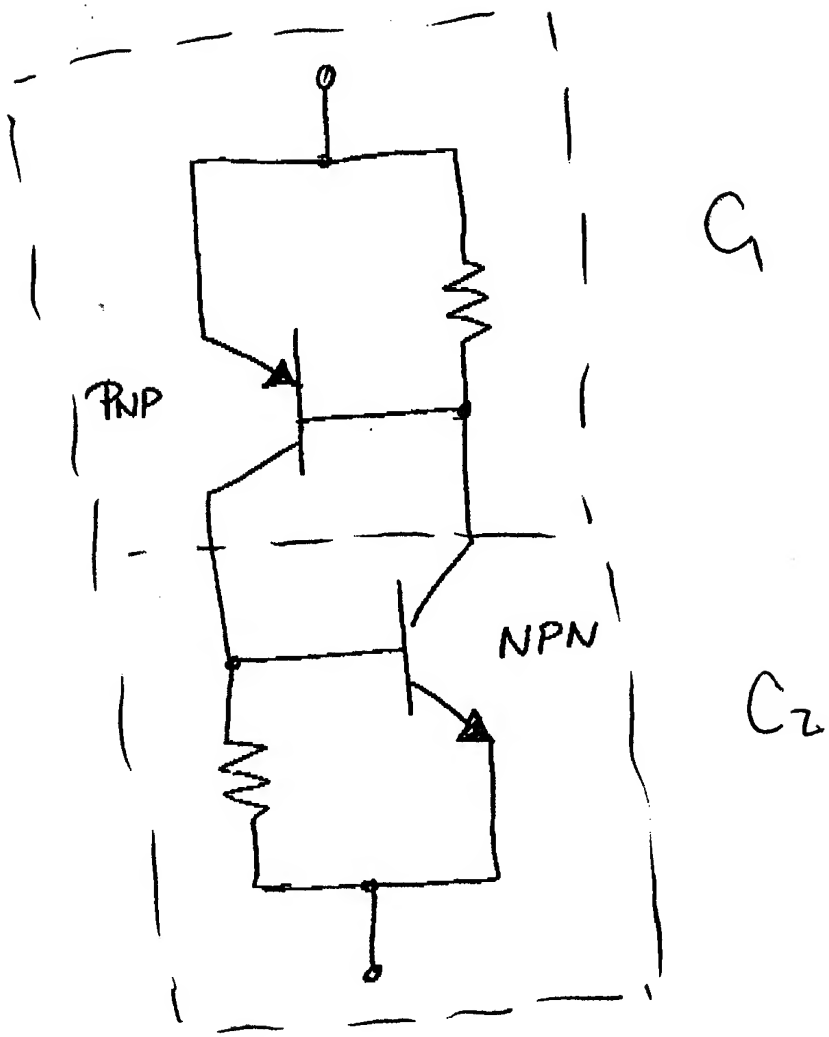

Figure 4

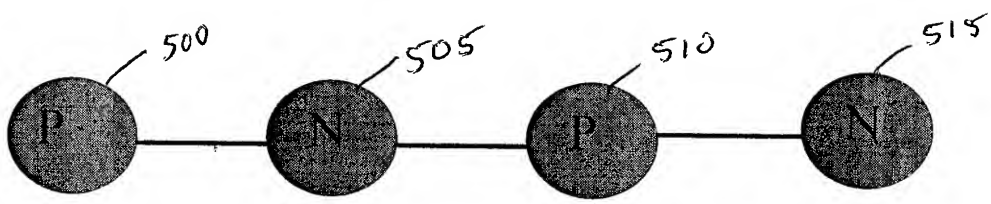

Figure 5. Graph Model

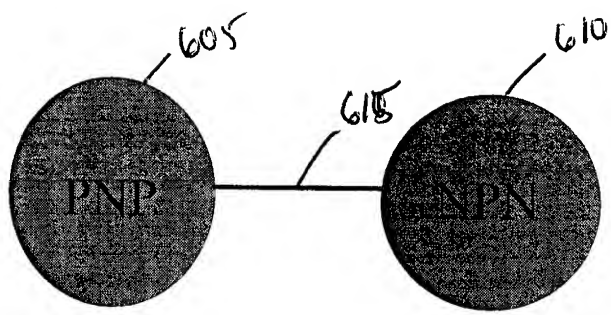

Figure 6. Graph Model

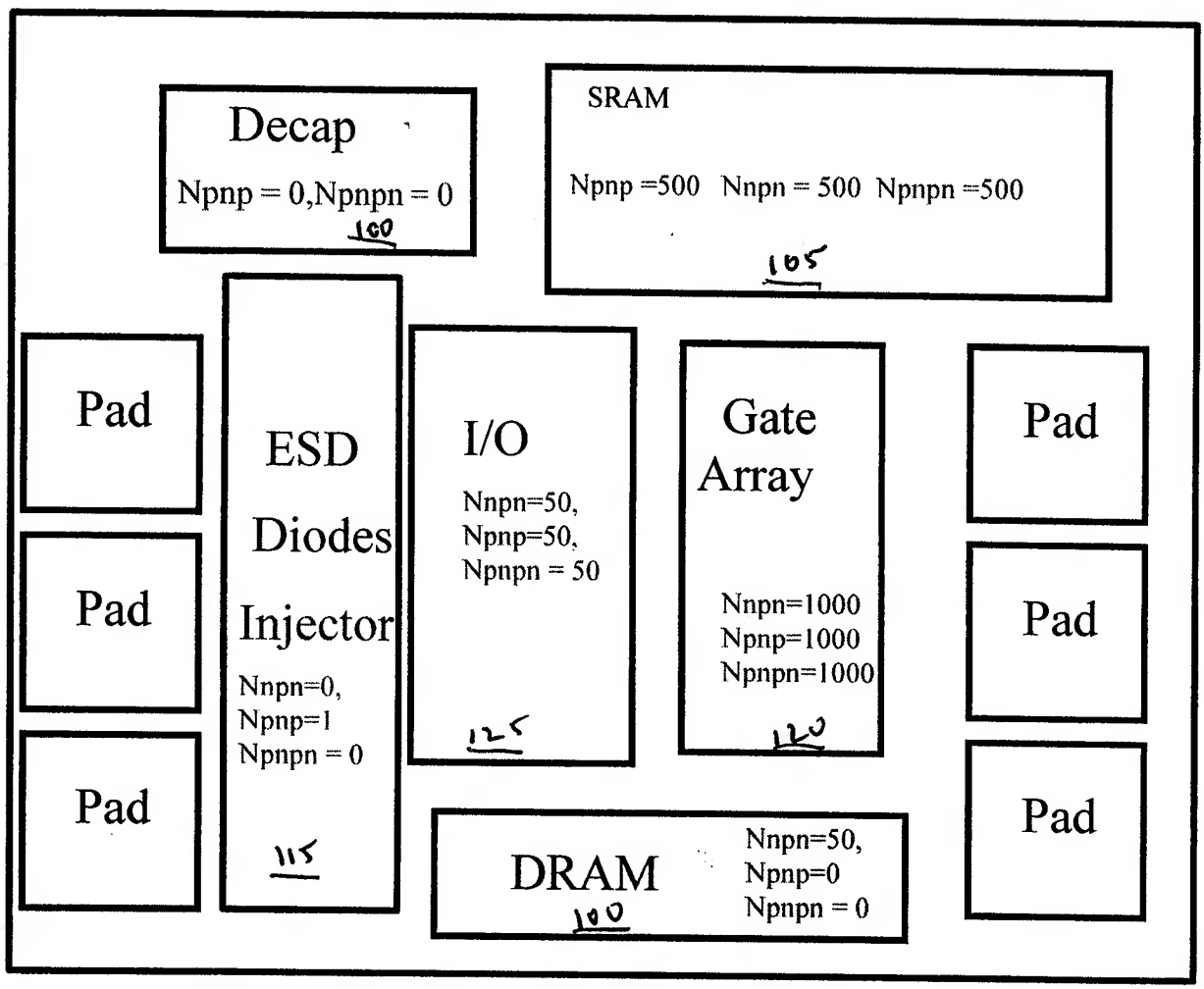
Decap
Npnp = 0,Npnpn = 0
100
SRAM
Npnp =500 Nnpn = 500 Npnpn =500
105
Pad
Pad
Pad
ESD
Diodes
Injector
Nnpn=0,
Npnp=1
Npnpn = 0
115
I/O
Nnpn=50,
Npnp=50,
Npnpn = 50
125
Gate
Array
Nnpn=1000
Npnp=1000
Npnpn=1000
120
Pad
Pad
Pad
DRAM
100
Nnpn=50,
Npnp=0
Npnpn = 0

Figure 7

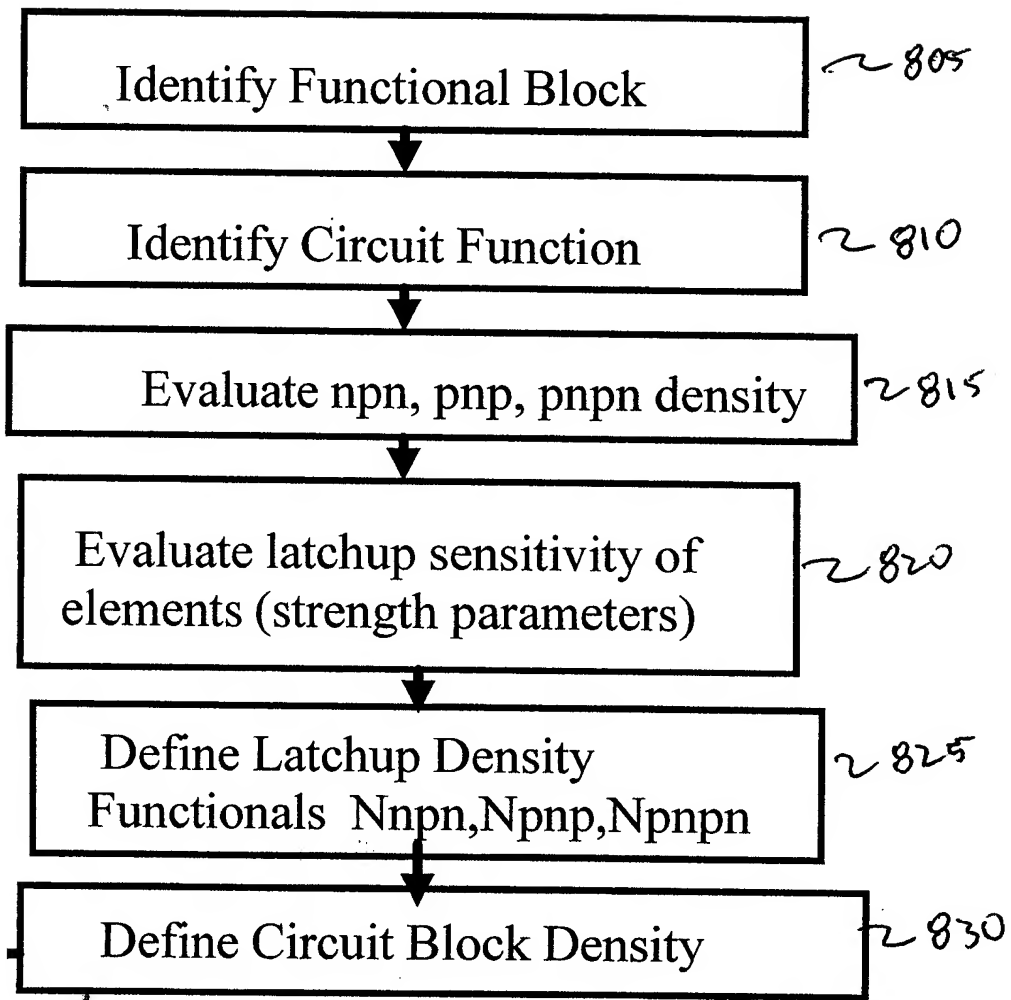

Figure 8 Method

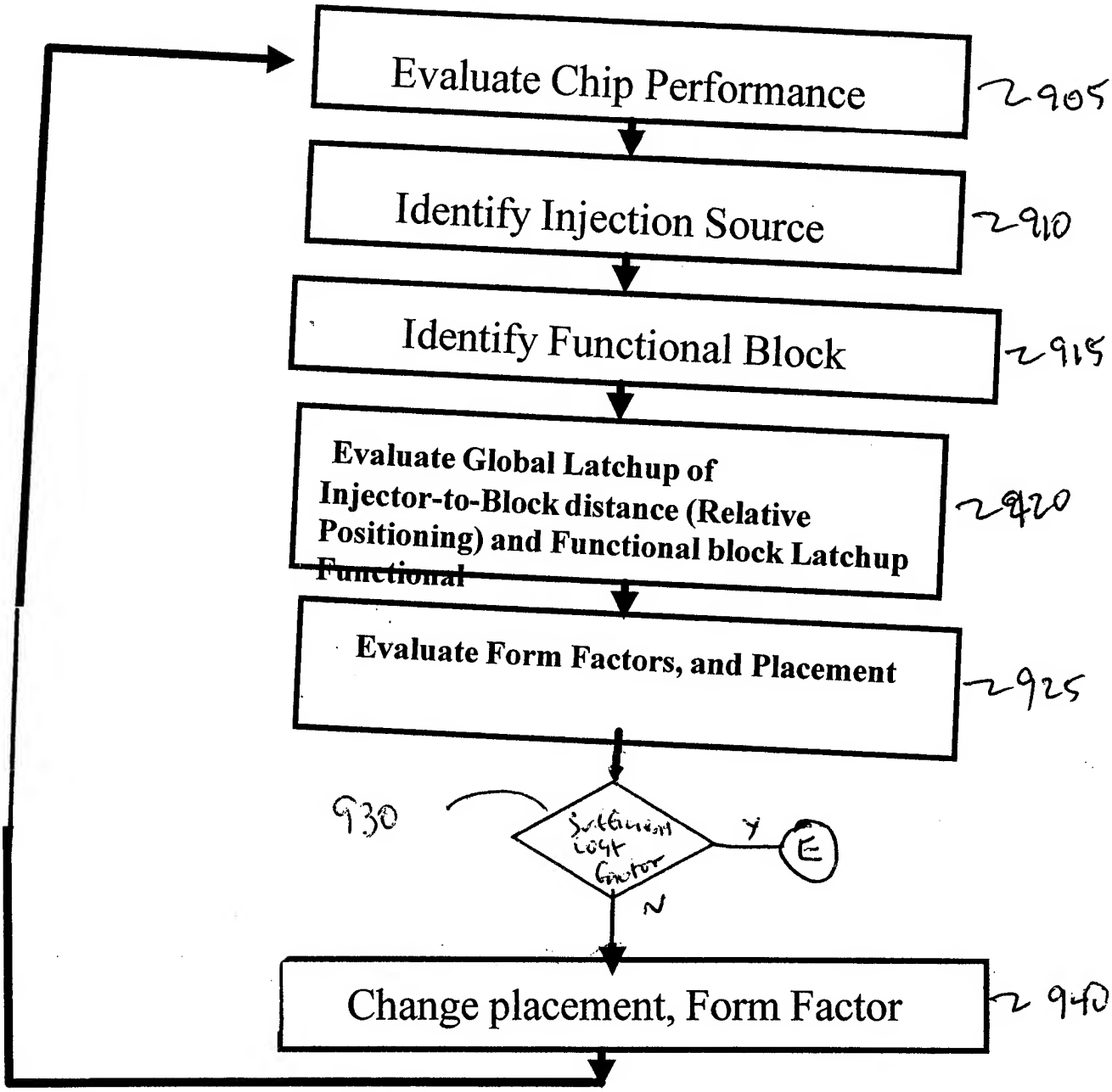
Evaluate Chip Performance
2905
Identify Injection Source
2910
Identify Functional Block
2915
Evaluate Global Latchup of Injector-to-Block distance (Relative Positioning) and Functional block Latchup Functional
2920
Evaluate Form Factors, and Placement
2925
930
Y
N
Change placement, Form Factor
2940

Figure 9